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A Novel Approach for the Correction of Cyclic Redundancy Check using Hybrid Matrix Code

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ABSTRACT: Communication involves transfer and reception of data. Errors must be introduced in the transmitted data due to external radiations and noise. So several approaches are used for error detection and correction. This paper proposes a novel approach were Cyclic Redundancy Check (CRC) is used for the error detection along with the Hybrid Matrix Code(HMC) for the correction of generated CRC value and they are coded in verilog HDL and simulated using Xilinx ISE Design suite 14.2.This proposed method can provide maximum error detection and correction capability with reduction in delay.

KEYWORDS: Cyclic Redundancy Check, Linear Feedback Shift Register, Look Up Table, Hybrid Matrix Code.

I. INTRODUCTION

Data communication basically involves transfer of data from one place to another or from one point of time to another. Error may be introduced by the channel which makes data unreliable for user. This introduced error should be detected, because error detection is essential for its correction. Hence we need different error detection and error correction schemes. The error detection basically uses the concept of redundancy. The most powerful redundancy based detection method is CRC. This method provide only error detection capability so in order to correct the errors, HMC is used. This paper deals with a novel method which uses a redundancy based error detection method namely Cyclic Redundancy Check (CRC) and incorporates a correction method namely Hybrid Matrix Code(HMC) that is used to correct the received CRC error. The rest of the paper is structured as follows: Section 2 deals with literature survey, section 3 deals with CRC and next section deals with HMC and section 5 explains the work done and conclude the paper in section 6.

II. LITERATURE SURVEY

Mainly there are two types of error in data communication. 1) single bit error 2) burst error[1]. In single bit error, only one bit get altered, whereas in case of burst error as its name indicate multiple bits get altered. The number of bits get altered is measured from the first corrupted bit to the last corrupted bit. There are several error detection methods which uses the concept of redundancy. They are

- Vertical Redundancy Check(VRC)
- Longitudinal Redundancy Check(LRC)
- Cyclic Redundancy Check(CRC)

VRC is also known as parity check. In case of VRC a single bit is appended along with the data block so as to make parity even or odd. By using this method it is possible to detect all single bit errors and also the burst errors if the total number of errors in each data unit is odd in case of even parity. In LRC [2] the incoming data block is organized in the form of table and the parity for each column is calculated. A longitudinal redundancy check (LRC) is a form of redundancy check that is applied independently to each of a parallel group of bit streams**.** This parity bits forms the redundant bit for the data block.LRC of n bit can detect a burst error of n bits. If two bits in one row data is changed, for the another row data also if the same bit position is altered, then it do not detect the error. The most powerful redundancy based error detection method is CRC. This method is based on polynomial division whereas the remaining methods are based on addition. Here instead of appending zeros, CRC remainder is appended as the redundant bits. By using this method, all burst errors equal to or less than the degree of the generator polynomial can be detected. By using this method also, only detection is possible. So several methods are used for the error detection.

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- Hamming code
- Built In Current Sensor Code
- Matrix Code

Hamming code is the linear block code which can detect and correct only single bit of error. Whereas in case of Built in Current Sensor (BICS) method, the error is detected by examine the variations in the current. It can combined with either hamming code or parity code. The BICS combined with hamming code can provide better reliability. The another set of error detection method is the matrix code where data is arranged in the form of matrix. The matrix code method can provide only two bit error correction capability. The different types of matrix code methods[8] are parity matrix code(PMC), hybrid matrix code(HMC), decimal matrix code(DMC). HMC can provide maximum error correction capability with less number of redundant bits, reduced delay and area overhead.

III. CYCLIC REDUNDANCY CHECK

The cyclic redundancy check, or CRC, is a technique for detecting errors in digital data, but not for making corrections when errors are detected. It is used primarily in data transmission. In the CRC method, a certain number of check bits, often called a checksum, are appended to the message being transmitted [3]. The incoming data stream is divided with a standard generator polynomial and the remainder obtained is the CRC. The receiver can determine whether or not the check bits agree with the data, to check weather an error is occurred or not. If an error occurred, the receiver sends a "negative acknowledgement" (NAK) back to the sender, requesting that the message be retransmitted. There are two ways to implement CRC.

- Serial CRC implementation
- Parallel CRC implementation

1. SERIAL CRC IMPLEMENTATION

Serial CRC Implementation is based on the concept of Linear Feedback Shift Register. LFSR is a combination of D flipflops and XOR gates. The general representation of an LFSR is shown in Figure 1. The incoming binary polynomial is represented in the form of a binary sequence in case of an LFSR. That is the coefficients of the binary sequence are considered. Based on the most significant bit (Coefficient) LFSR performs a single bit shift operation or single bit shift and XOR operation. If the coefficient bit is zero it perform the shift operation and in the else case it first perform the XOR operation with the generator polynomial before it get shifted. In serial CRC, only one bit is treated during one clock cycle [4]. So the throughput is less.

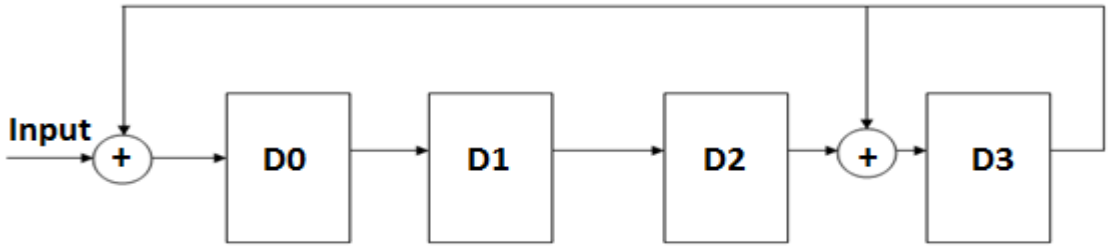

Fig. 1: General representation of LFSR

2. PARALLEL CRC IMPLEMENTATION

In parallel CRC implementation multiple bytes are considered during one clock cycle.To accelerate parallel CRC implemenation several algorithms are used. The commonly used algoritms are:

- Sarwate algorithm
- Slicing by N algorithm

In Sarwate algorithm, a single look up table is used to store all the possible combinations of input value. For example, suppose if we have 128 bit input value, it have a possibility of 2^{128} combinations and all these values are stored in a single look up table and as a result the LUT become large. Thus it requires more memory usage. In case of Slicing by N

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algorithm (N=4, 8, 16, 32) instead of using a single look up table, multiple look up tables are used. So less memory usage compared with Sarwate method. This is the main advantage of the slicing by N algorithm when compared to that of the slicing algorithm [6]. The parallel CRC implementation with multiple look table method is used for the CRC-64 generation.

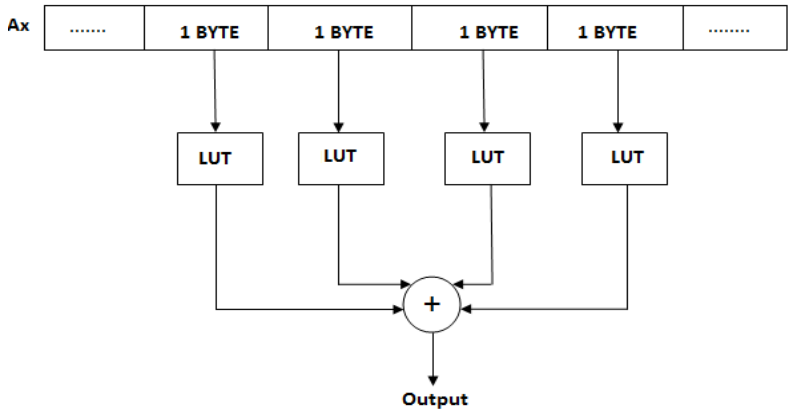

Fig. 2: Zero block look up tables

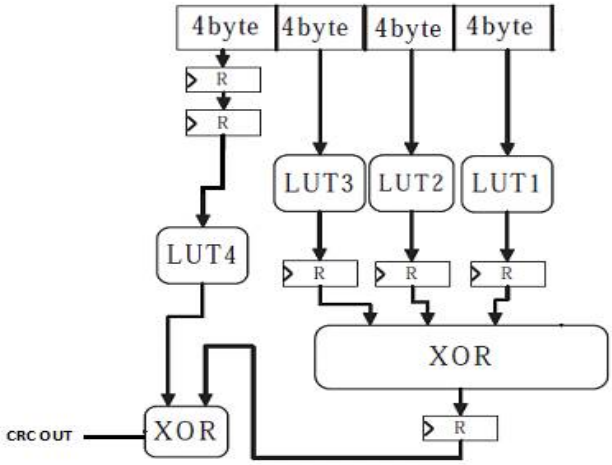

Fig. 3: Parallel CRC implementation

In Slicing by 4 algorithm, the incoming 128 bit of data is taken and it is XORed with the initial CRC value. The initial CRC-64 value used here is the 0xFFFFFFFFFFFFFFFF.This modified bit stream is divided into four slices where each slice consist of 4 bytes of data. These four bytes of data is again divided into four single bytes as shown in figure 2 and all the possible values for each byte is precomputed by using the LFSR based method and stored in the corresponding LUT's. The final CRC value for each slice is obtained by XORing all the LUT values. The same operation is repeated for all the other slices. The final CRC-64 is generated by perform the XOR operation between the four LUT's as in figure3 [7]. The standard generator polynomial should be chosen in such a way that it provide maximum error correction capability. The standard polynomial used for the CRC generation is given by the polynomial:
$G(x)=X^{64}+X^{52}+X^{46}+X^{44}+X^{32}+X^{26}+X^{23}+X^{22}+X^{16}+X^{12}+X^{11}+X^{10}+X^{8}+X^{7}+X^{5}+X^{4}+X^{2}+X+1$.CRC is used only for the error detection.so in order to correct the received CRC error,different error correction methods are used.Among the different possible error correction methods HMC is used because of reduced redundant bits and area due to the encoder reuse technique.

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IV. HYBRID MATRIX CODE

HMC is the combination of the hamming code and the matrix code.This error correction method operates on the basis of the hamming code algorithm so as to provide better error correction capability.

1. HMC ENCODER

In the encoder section, the incoming data stream is arranged in the form of a matrix that means it consist of horizontal rows and vertical columns. The incoming N bit word is divided into k symbols with m bits. Then the horizontal redundant bits are generated by performing the hamming code operation between symbol 0 and symbol 2 and also between the other symbols per row as shown in figure 4. The vertical redundant bits are generated by performing the binary operation between D0 and D16 and also between the other bits in the vertical column [9].

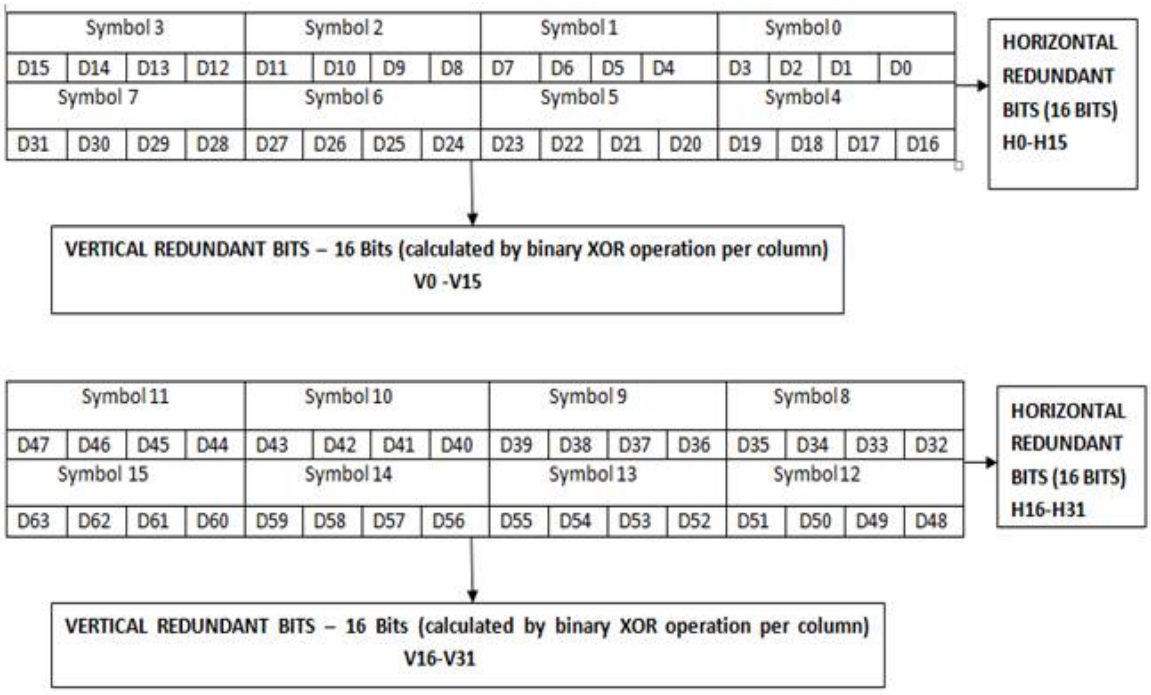

Fig. 4: HMC Encoder

2. HMC DECODER

In order to obtain the correct code word, the decoder section is required. It consist of syndrome calculator, error detector and error corrector section. The decoder section generates the received redundant bits by using the received information bits. Then by performing the binary operation between the redundant bits and the received redundant bits the syndrome bits are generated. Thus horizontal and vertical syndrome bits are generated. If the horizontal syndrome bit is zero, then there is no error else an error is occurred. Then by checking which vertical syndrome bit is non zero, the corresponding error bit can be found out. If the horizontal syndrome bits are zero, and a non zero value corresponds to any of the vertical syndrome bits represents an error in the second row of data bits. Then the error corrector can correct the induced errors. Thus this method provide method maximum error correction capability with less number of redundant bits.

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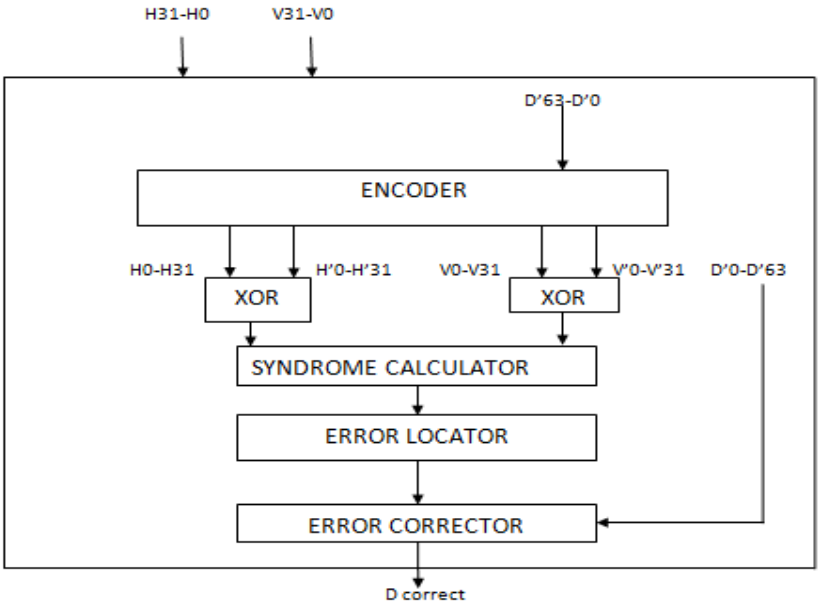

Fig. 5: HMC Decoder

V. WORK DONE

Serial and parallel CRC-64 implementation is done for 128 bit of input data. The serial implementation is done by using the LFSR based method and the parallel implementation by using Slicing by 4 algorithm. A comparative study is done between these two methods on the basis of delay and area. But by using this method only error detection is possible. So in order to correct the received CRC error, Hybrid Matrix Code method is also incorporated into the CRC based error detection. Thus both error detection and correction is done by using this method.

5.1 SIMULATION RESULTS

Analysis were done on Xilinx ISE design suite 14.2.FPGA used is SPARTAN3E, xc3s500e-5ft256 device is considered.

Table 1: Delay Analysis

Method	Delay(ns)
LFSR	7.08
LUT	6.93

Table 2: Logic Utilization

Method	Number of slices(4656)	Number of 4 input lut's(9312)
LFSR	876	1450
LUT	2626	5612

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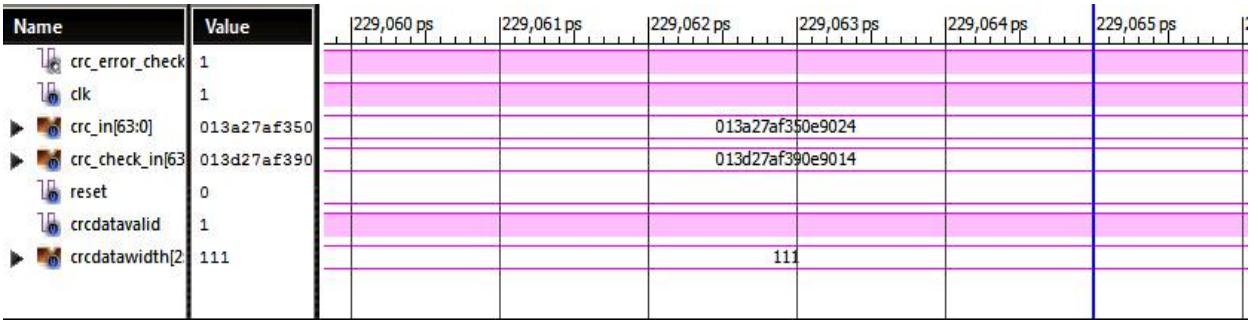

Fig. 6: CRC generation using LFSR

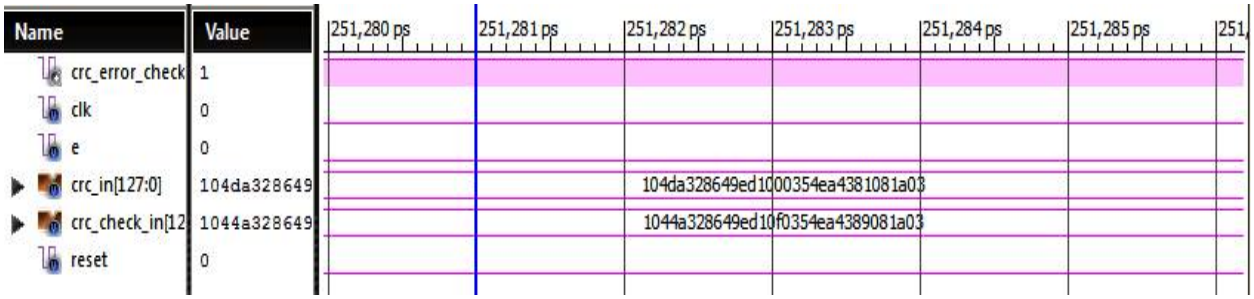

Fig. 7: CRC generation using LUT

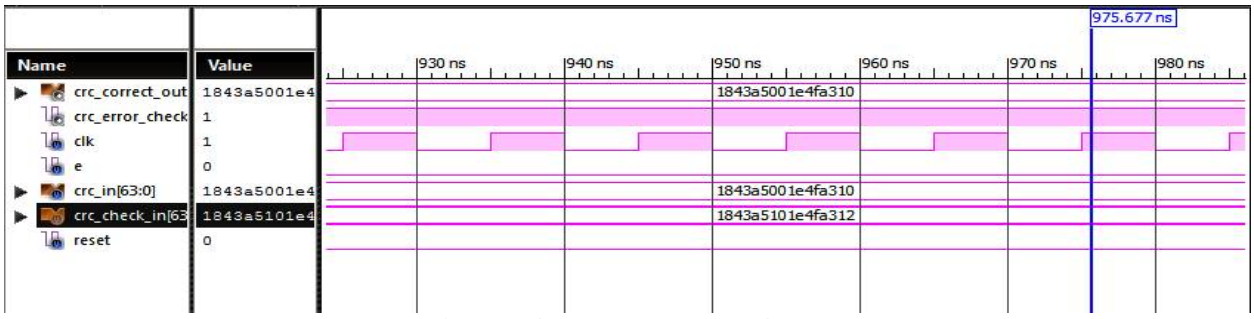

Fig. 8: Error Correction using HMC

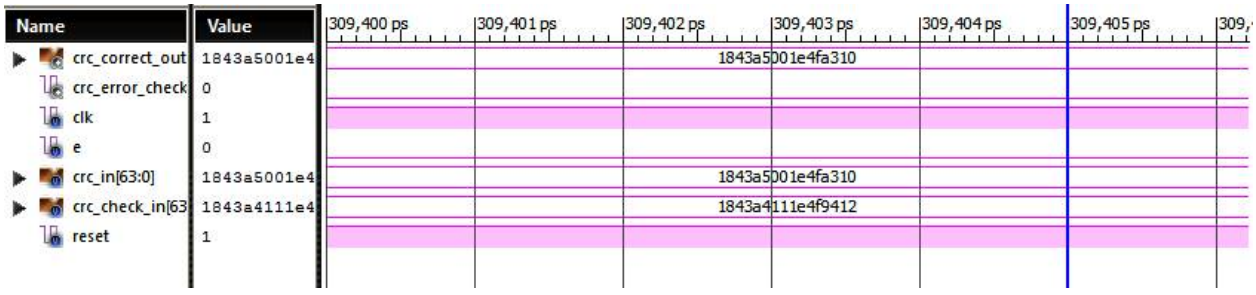

Fig. 9: CRC error correction using HMC

VI. CONCLUSION

64 bit CRC implementation is done for 128 bit of input data in both serial and parallel manner and a comparative study is done between these two methods and arrived at a conclusion that parallel CRC implementation is the better choice for the CRC implementation. The CRC is used only for the error detection, so here incorporates an error correction

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method that is the Hybrid Matrix Code method. The result demonstrates that Cyclic Redundancy Check is useful for error detection and Hybrid Matrix Code for error correction with reduced area utilization by the reuse of the encoder section and delay overhead. This paper incorporates an efficient error detection and correction method for the reliable communication over noisy channel.

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